REMARKS

Claim 1 has been amended to provide proper antecedent basis for the term "input signal."

Applicant notes with appreciation the finding that claims 2-4, 7-9, 12, 14, 16 and 18 would be allowable if redrafted in independent form. However, those claims have not been redrafted because it is believed that the base claims are allowable as discussed below.

Claims 1, 5-6, 10-11, 13, 15 and 17 were rejected under 35 U.S.C. 102(e) as being anticipated by Tateishi et al. (6,097,777). That rejection is respectfully traversed and reconsideration is requested.

As discussed in prior responses, and with reference to Figure 14, the present invention relates to a frequency generating circuit which generates an output signal bclk at a rate that is a multiple of an input signal aclk. To that end, a phase comparator 191 directly compares the phase of an edge of an input signal with the phase of an edge of the output signal, that is, through the top feedback loop of Figure 14. Prior art circuits such as illustrated in Figure 16 have not directly compared the two signals but, rather, have inserted a divider 193 between the output and the phase comparator.

The Tateishi et al. circuit operates in three modes, none of which anticipates any claim of the present invention.

In a first mode indicated in Fig. 4 between times t_1 and t_2 and between t_6 and t_7, the input to the phase locked loop (PLL) circuit 6 is selected as signal r from the reference crystal oscillator. In that mode, the phase frequency comparator 60A is selected, so feedback is through the frequency divider 65. See column 6, lines 47-63. From the discussion of mode 2, it is understood that the reproduced clock would have a rate that is an N times multiple of the output of the edge detector 66. Thus, in that mode, the output is a multiple of an input frequency, but the output is not directly compared to an input since the output passes through the divider 65.

In second and third modes of operation, the input is taken from the DVD pick up 1. In the second mode of operation, for example between times t_2 and t_4, the data which is received is, like the signal r, repetitive with a transition every four time units. In this mode, the PFC 60A is again selected, so the output passes through the frequency divider 65. See column 7, lines 43-55. Again in this second mode, the PLL multiplies by N, but the phase comparator does not directly compare phase of an input signal with that of an output signal.

The third mode is during the receipt of random data such as between t_4 and t_5 and during the data signal before time t_8. During this mode, the output signal from the VCO 64 is applied directly to a phase comparator 60B (column 7, lines 56-67), and it is this phase comparator to which the Examiner refers. However, during this mode of operation, the incoming data stream from the pick-up 1 has transitions that are separated by periods ranging from 3 to 11 time units (column 5, lines 58-62). The VCO 64 does not respond by generating a reproduced clock at a rate that is a multiple of that random frequency signal. Rather, the previously set frequency is maintained, and operation of the PC type circuit, illustrated at the bottom of Figure 4, allows phase lock to those random transitions without requiring that the output be a multiple of the input frequency.

Thus, in the modes during which the circuit of Tateishi et al. could be said to be a multiplier circuit having a frequency generating circuit which generates an output signal that is a multiple of an input frequency, that is, the first and second modes, the phases of the input and output signals are not directly compared. On the other hand, where there is direct comparison, the circuit does not function as a multiplier circuit with a frequency generating circuit which generates an output at a rate that is a multiple of an input frequency.

With respect to claims 13, 15 and17, there is no mention in the Tateishi et al. patent of using a combinational phase comparator, nor of using transistors to build such a comparator.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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